IN THE CLAIMS:

1. (Currently Amended) A ferroelectric memory device comprising;

a plurality of ferroelectric ~~capacitor~~ capacitors, each including a top electrode, a common bottom electrode and a ferroelectric film interposed ~~between the top and bottom electrodes, the top electrode having a rectangular planar pattern~~ therebetween;

a plurality of memory cell ~~transistor~~ transistors, each including first and second doped layers and a gate, ~~the~~ each of said plurality of memory cell ~~transistor~~ transistors controlling a voltage supplied to the top electrode of ~~the~~ a corresponding ferroelectric capacitor;

a first interlevel dielectric film formed over the plurality of memory cell ~~transistor~~ transistors and the plurality of ferroelectric ~~capacitor~~ capacitors; and

a ~~first~~ plurality of interconnection ~~layer~~ layers formed on the first interlevel dielectric film, each of the plurality of interconnection layers electrically connecting a memory cell transistor to a corresponding ferroelectric capacitor; ~~and~~

~~a memory cell composed of the ferroelectric capacitor and the memory cell transistor,~~

wherein, in a ~~planar layout~~ plan view of the ferroelectric memory device, ~~the first interconnection layer partially overlaps with the top and bottom electrodes of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode and the bottom electrode~~ all interconnection layers formed on the first interlevel dielectric film and electrically connecting a respective memory cell transistor to a corresponding ferroelectric capacitor, extend over a same side of the common bottom electrode and only one side of a corresponding top electrode, and the width of a bit line formed above ~~the~~ a respective top electrode is smaller than the distance between the respective top electrode and ~~another top electrode adjacent to the~~ an adjacent top electrode[[;]]

~~wherein the memory cell comprises a memory cell array arranged in a matrix,~~

~~wherein the first interconnection layer extends in a same direction orthogonal to the extending direction of the bottom electrode, not extending in an opposite direction, with respect to the top and bottom electrodes, and~~

~~wherein a plurality of the top electrodes is arranged only in a row with respect to the direction of the length of the bottom electrode~~.

2. (Currently Amended) The device of Claim 1, wherein ~~the first~~ each of the plurality of interconnection ~~layer~~ layers includes:

a storage line connected to the top electrode of the corresponding ferroelectric capacitor and to the first doped layer of the corresponding memory cell transistor, the storage line having a linear planar pattern; and

a bit line connected to the second doped layer of the corresponding memory cell transistor, and

wherein the storage line intersects only one side of the top electrode in the planar layout.

3. (Currently Amended) The device of Claim 2, wherein the storage line includes:

a first region connected to the top electrode of the corresponding ferroelectric capacitor;

a second region connected to the first doped layer of the corresponding memory cell transistor; and

a third region being interposed between the first and second regions and intersecting the side of the top electrode in the planar layout, and

wherein the line width of the third region is smaller than that of the first and second regions.

4. (Original) The device of Claim 2, wherein the bit line does not overlap with the top electrode in the planar layout.

5. (Currently Amended) The device of Claim 4, wherein the storage line includes:

a first region connected to the top electrode of the corresponding ferroelectric capacitor;

a second region connected to the first doped layer of the corresponding memory cell transistor; and

a third region being interposed between the first and second regions and intersecting the side of the top electrode in the planar layout, and

wherein the line width of the third region is smaller than that of the first and second regions.

6. (Currently Amended) The device of Claim 1, wherein ~~the first~~ each of the plurality of interconnection ~~layer~~ layers includes:

a storage line connected to the top electrode of the corresponding ferroelectric capacitor and to the first doped layer of the corresponding memory cell transistor, the storage line having a linear planar pattern; and

a bit line connected to the second doped layer of the corresponding memory cell transistor, and

wherein the bit line does not overlap with the top electrode in the planar layout.

7. (Currently Amended) The device of Claim 1, wherein ~~the first~~ each of the plurality of interconnection ~~layer~~ layers is made of a material containing at least one of aluminum and copper.

8. (Currently Amended) The device of Claim 1, further comprising:

an upper interlevel dielectric film formed to cover ~~the first~~ each of the plurality of interconnection ~~layer~~ layers; and

an upper interconnection layer formed on the upper interlevel dielectric film,

wherein the ~~second~~ upper interconnection layer totally covers the top electrode of the corresponding ferroelectric capacitor in the plan view [[planar layout]].

9. (Currently Amended) The device of Claim 1, further comprising:

an upper interlevel dielectric film formed to cover ~~the first~~ each of the plurality of interconnection ~~layer~~ layers; and

an upper interconnection layer formed on the upper interlevel dielectric film,

wherein the ~~second~~ upper interconnection layer totally covers the bottom electrode of the corresponding ferroelectric capacitor in the plan view [[planar layout]].

10. (Currently Amended) The device of Claim 9, wherein the ~~second~~ upper interconnection layer is made of a material containing at least one of aluminum and copper.

11. (Currently Amended) The device of claim 8, wherein the ~~second~~ upper interconnection layer is made of a material containing at least one of aluminum and copper.

12. (Previously Added) A ferroelectric memory device comprising;

a ferroelectric capacitor including a top electrode, a bottom electrode and a ferroelectric film interposed between the top and bottom electrodes, the top electrode having a rectangular planar pattern;

a memory cell transistor including first and second doped layers and a gate, the memory cell transistor controlling a voltage supplied to the top electrode of the ferroelectric capacitor;

a first interlevel dielectric film formed over the memory cell transistor and the ferroelectric capacitor;

a first interconnection layer formed on the first interlevel dielectric film; and

a memory cell composed of the ferroelectric capacitor and the memory cell transistor,

wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode;

wherein the memory cell comprises a memory cell array arranged in a matrix,

wherein the first interconnection layer extends only in one direction with respect to the top and bottom electrodes, and

wherein a plurality of the top electrodes is arranged only in a row with respect to the direction of the length of the bottom electrode,

wherein the first interconnection layer includes:

a storage line connected to the top electrode of the ferroelectric capacitor and to the first doped layer of the memory cell transistor, the storage line having a linear planar pattern; and

a bit line connected to the second doped layer of the memory cell transistor, and

wherein the storage line intersects only one side of the top electrode in the planar layout, and

wherein the storage line includes:

a first region connected to the top electrode of the ferroelectric capacitor;

a second region connected to the first doped layer of the memory cell transistor; and

a third region being interposed between the first and second regions and intersecting the side of the top electrode in the planar layout, and

wherein the line width of the third region is smaller than that of the first and second regions.

13. (Previously Added) The device of Claim 12, wherein the bit line does not overlap with the top electrode in the planar layout.

14. (Cancelled).

15. (Currently Amended) A ferroelectric memory device comprising.

a plurality of ferroelectric ~~capacitor~~ capacitors, each including a top electrode, a common bottom electrode and a ferroelectric film interposed ~~between the top and bottom electrodes, the top electrode having a rectangular planar pattern~~ therebetween;

a first interlevel dielectric ~~films~~ film formed over the plurality of ferroelectric ~~capacitor~~ capacitors; and

a ~~first~~ plurality of interconnection ~~layer~~ layers formed on the first interlevel dielectric film,

wherein, in a ~~planar layout~~ plan review of the ferroelectric memory device, ~~the first interconnection layer partially overlaps with the top and bottom electrodes of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode and the bottom electrode~~ all interconnection layers formed on the first interlevel dielectric film extend over a

same side of the common bottom electrode and only one side of a corresponding top electrode, and the width of a bit line formed above ~~the~~ a respective top electrode is smaller than the distance between the respective top electrode and ~~another top electrode adjacent to the~~ an adjacent top electrode[[;]]

~~wherein the first interconnection layer extends in a same direction orthogonal to the extending direction of the bottom electrode, not extending in an opposite direction, with respect to the top and bottom electrodes, and~~

~~wherein a plurality of the top electrodes is arranged only in a row with respect to the direction to the length of the bottom electrode~~.

16. (Currently Amended) The device of Claim 15, wherein ~~the first~~ each of the plurality of interconnection ~~layer~~ layers is made of a material containing at least one of aluminum and copper.

17. (New) The device of Claim 1, wherein the ferroelectric memory device comprises a plurality of memory cells arranged in a matrix, each of the plurality of memory cells comprises a respective ferroelectric capacitor and a corresponding memory cell transistor.

18. (New) The device of Claim 1, wherein each of the plurality of interconnection layers extends in a direction orthogonal to the longitudinal direction of the common bottom electrode.

19. (New) The device of Claim 1, wherein each of the plurality of interconnection layers is electrically connected to a corresponding memory cell transistor by a first contact and to a corresponding ferroelectric capacitor by a second contact.

20. (New) The device of Claim 1, wherein each of the plurality of top electrodes has a rectangular planar pattern.

21. (New) The device of Claim 1, wherein the plurality of ferroelectric capacitors, the plurality of memory cell transistors, the first interlevel dielectric film and the plurality of interconnection layers form a row of an array of the ferroelectric memory device, and

the array of the ferroelectric memory device comprises a plurality of the rows.